

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter to each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of  
sole or first inventor: KLAS E. FRIEDMAN

Inventor's Signature: [Signature]

Date: 4/17/87

Residence: 243 Mistletoe Road  
Los Gatos, California 95030

Citizenship: Finland

Post Office Address: 243 Mistletoe Road  
Los Gatos, California 95030

PIF 00029

041994

Applicant or Patentee: KLAS H. EKLUND Attorney's  
 Serial or Patent No.: \_\_\_\_\_ Pocket No.: 520-01  
 Filed or Issued: \_\_\_\_\_  
 For: HIGH VOLTAGE MOS TRANSISTORS

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS  
 (37 CFR 1.9(f) and 1.27(c) - INDEPENDENT INVENTOR)

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled HIGH VOLTAGE MOS TRANSISTORS described in

☒ the specification filed herewith  
☐ application serial no. \_\_\_\_\_, filed \_\_\_\_\_  
☐ patent no. \_\_\_\_\_, issued \_\_\_\_\_

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

☒ no such person, concern, or organization  
☐ persons, concerns or organizations listed below:

\*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention asserting to their status as small entities. (37 CFR 1.27)

FULL NAME n/a  
 ADDRESS \_\_\_\_\_  
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME n/a  
 ADDRESS \_\_\_\_\_  
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME n/a  
 ADDRESS \_\_\_\_\_  
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

KLAS H. EKLUND  
 NAME OF INVENTOR \_\_\_\_\_ NAME OF INVENTOR \_\_\_\_\_  
 Signature of Inventor \_\_\_\_\_ Signature of Inventor \_\_\_\_\_  
4/17/87 \_\_\_\_\_  
 Date \_\_\_\_\_ Date \_\_\_\_\_

PIF 00030

041994

KLAS H. EKLUND

SS-520-01

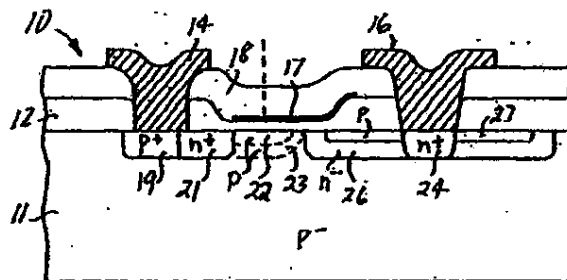


Fig. 1

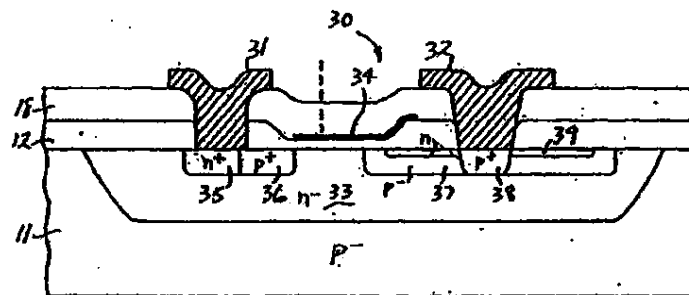


Fig. 2

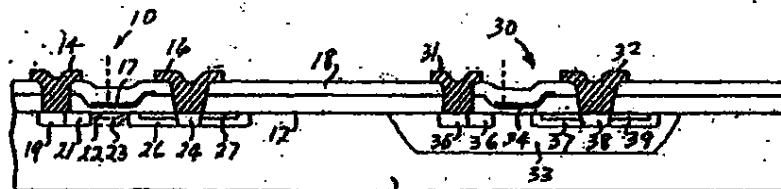


Fig. 3

SE-2

6mm p 250

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KLAS H. EKLUND

SS-520-01

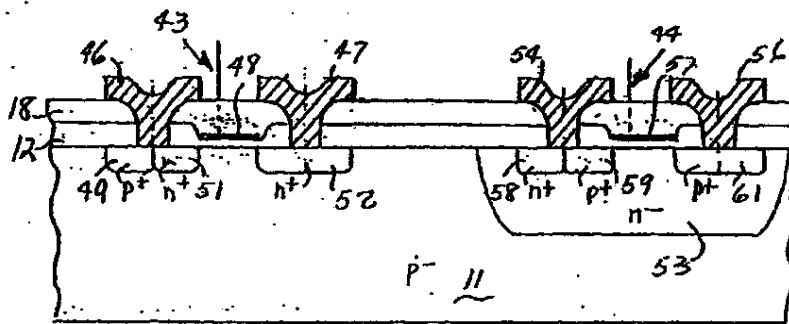


Fig. 4

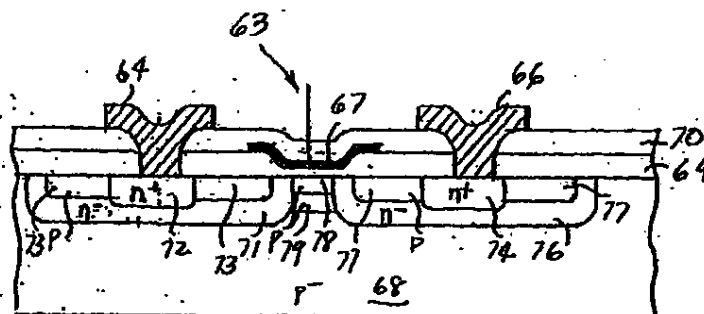


Fig. 5

PIF 00032

UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark OfficeAddress: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY/AGENT NO.
07/041,994	04/24/87	ERLUND	00-920-81

THOMAS E. SCHATZEL  
3211 SCOTT BLVD., STE. 201  
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON, S. J.	
ART UNIT	PAPER NUMBER
253	2

DATE MAILED: 12/07/87

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☐ Responsive to communication filed on ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 months, — days from the date of this notice.  
Failure to respond within the period for response will cause the application to become abandoned, 35 U.S.C. 131

## Part I THE FOLLOWING ATTACHMENTS ARE PART OF THIS ACTION:

- |   |   |
|---|---|
| 1. <input checked="" type="checkbox"/> Notice of References Cited by Examiner, PTO-402. | 2. <input checked="" type="checkbox"/> Notice re Patent Drawing, PTO-606.       |
| 3. <input type="checkbox"/> Notice of Art Cited by Applicant, PTO-549                   | 4. <input type="checkbox"/> Notice of Informal Patent Application, Form PTO-532 |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474      | 6. <input type="checkbox"/> _____   |

## Part II SUMMARY OF ACTION

1. ☒ Claims 1-18 are pending in the application.  
Of the above, claims \_\_\_\_\_ are withdrawn from consideration.
2. ☐ Claims \_\_\_\_\_ have been cancelled.
3. ☐ Claims \_\_\_\_\_ are allowed.
4. ☒ Claims 1-18 are rejected.
5. ☐ Claims \_\_\_\_\_ are objected to.
6. ☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on \_\_\_\_\_. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_ has (have) been ☐ approved by the examiner, ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed \_\_\_\_\_, has been ☐ approved, ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are correct. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received  
☐ been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1956 C.D. 31; 453 O.G. 253.
14. ☐ \_\_\_\_\_

PTOL-226 (Rev. 7-82)

EXAMINER'S ACTION

PIF 00033

Serial No. 041,994

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Art Unit 253

On page 9 line 28 "72" should be --73--.

Claims 1, 2, 4-7, 16 are rejected under 35 U.S.C. 112, first and second paragraphs, as the claimed invention is not described in such full, clear, concise and exact terms as to enable any person skilled in the art to make and use the same, and/or for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The structure of claim 1 is indefinite. The language "being united in one structure" is vague and indefinite and does not clearly or concretely define the structure of applicant's invention. The terms "insulated gate FET" and "double sided JFET" are also broad and do not define applicant's invention. Claim 2 is confusing since lines 14-17 mimic lines 17-20. The other claims are rejected for dependence on 1 or 2.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP 608.01(o). Correction of the following is required: there is no proper antecedent in the specification for the process descriptions of claims 11, 13, 14, 17.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international

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Serial No. 041,994

-3-

Art Unit 253

application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-3, 5-9, 11, 12, 16 rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak.

Colak shows a CMOS device wherein layer 16 may perform the function of a JFET gate "on top of" an extended drain region 14 in the embodiment of figs. 2B or 2C. Substrate layer 12 may act as the other gate of the JFET. Clearly claim 1 does not distinguish over Colak. Note that mere labels as "JFET" do not structurally distinguish the claims over Colak since the structure of Colak may be labeled as IGFET in series with a double sided JFET as shown above. Claim 2 also does not distinguish over Colak since the claimed structure is shown in Colak and the intended use language "whereby current flow..." in claim 2 does not structurally distinguish over Colak and furthermore Colak's device may perform the same intended function. See *In re Pearson* 181 USPQ 642 or *Ex parte Minks* 169 USPQ 120 on statements of intended use in claims drawn to structure as we have here. Similarly claim 3 does not distinguish over Colak. Claim 5 is a product by process claim which does not structurally distinguish applicant's final product over Colak.

A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re*

PIF 00035

Serial No. 041,994

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Art Unit 253

Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by Process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim 6 also is undistinguishing over Colak since the thickness of layer 16 is a design variable and 1 micron thickness would not be unobvious to one of ordinary skill in view of Colak. Similarly, in re claim 7 a dopant density of greater than  $5 \times 10^{16}/\text{cc}$  would not be unobvious for the doping density of layer 16 of Colak. Claims 8, 9 also are obvious over Colak. Claims 11, 12 are product by process claims which also do not distinguish the final product over Colak. Claim 16 also does not distinguish over Colak as "floating" is vague and undistinguishing.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at

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Serial No. 042,994

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Art Unit 253

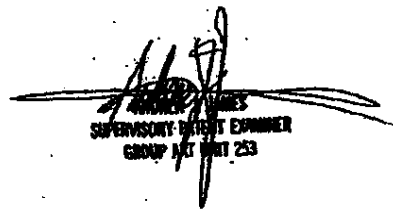
the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 4, 10, 13-15, 17 and 18 rejected under 35 U.S.C. 103 as being unpatentable over Colak in view of Thomas.

Thomas shows the obvious<sup>ness</sup> of providing low voltage and high voltage devices on the same substrate. It would be obvious from Thomas to practice Colak as CMOS or with other devices. Claim 4 is hence obvious. In re claims 10, 13, 15 "wall" regions are also obvious from Thomas. Claims 14, 17 also are product by process claims which do not distinguish the final product over the suggestions of the references on final structure. Claim 18 also does not distinguish over the suggestions of Colak in view of Thomas.

Any inquiry concerning this communication should be directed to J. Jackson at telephone number 783-557-4824.

  
Jackson/EH  
12-2-87

  
SUPERVISORY PATENT EXAMINER  
GROUP ART UNIT 253

PIF 00037

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND DISCARD CARBON

FORM PTO-892 (REV. 5-78)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. <b>041994</b>	GROUP/ART UNIT <b>253</b>	ATTACHMENT TO PAPER NUMBER <b>2</b>	
NOTICE OF REFERENCES CITED				APPLICANT(S) <b>Eklund</b>			
U.S. PATENT DOCUMENTS							
	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILED DATE IF APPROPRIATE	
A	4626879	12/86	Colak	387	23.8	12/82	
B	4628371	12/86	Thomas	357	23.8	9/85	
C							
D							
E							
F							
G							
H							
I							
J							
K							
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT DATE - I.P. DATE - P.T.
L							
M							
N							
O							
P							
Q							
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)							
R							
S							
T							
U							
DRAWN BY	DATE						
<b>J. Jackson</b>	<b>11/87</b>						

\* A copy of this reference is not being furnished with this office action.  
 From Manual of Patent Examination Procedures section 717.05 (a.)

PIF 00038

PTO - 918  
Rev. 8-92U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTACHMENT TO PAPER NUMBER	2
S.N.	41994

GROUP 260

## NOTICE OF PATENT DRAWINGS OBJECTION

Drawing Corrections and/or new drawings may only be submitted in the manner set forth in the attached letter, "Information on How to Effect Drawing Changes" PTO-1474.

- A. ☒ The drawings, filed on 4/24/08, are objected to as informal for reason(s) checked below:
- |   |  |
|---|--|
| 1. <input type="checkbox"/> Lines Faint.  | 11. <input type="checkbox"/> Parts in Section Must Be Hatched.   |
| 2. <input type="checkbox"/> Paper Poor.   | 12. <input type="checkbox"/> Solid Black Objectionable.  |
| 3. <input checked="" type="checkbox"/> Nomenclature Poor.                         | 13. <input type="checkbox"/> Figure Legends Placed Incorrectly.  |
| 4. <input checked="" type="checkbox"/> Lines Rough and Blurred.<br><u>FIG 1-5</u> | 14. <input type="checkbox"/> Mounted Photographs.  |
| 5. <input type="checkbox"/> Shade Lines Required.                                 | 15. <input checked="" type="checkbox"/> Extraneous Matter Objectionable.<br>[37 CFR 1.34 (1)]<br><u>BORDER LINES</u>   |
| 6. <input type="checkbox"/> Figures Must Be Numbered.                             | 16. <input type="checkbox"/> Paper Undersized; either 11" x 14",<br>or 21.6 cm x 29.7 cm. required.  |
| 7. <input type="checkbox"/> Heading Space Required.                               | 17. <input type="checkbox"/> Proper A4 Margins Required:<br><input type="checkbox"/> TOP 2.5 cm. <input type="checkbox"/> RIGHT 1.5 cm.<br><input type="checkbox"/> LEFT 2.5 cm. <input type="checkbox"/> BOTTOM 1.9 cm. |
| 8. <input type="checkbox"/> Figures Must Not Be Connected.                        | 18. <input type="checkbox"/> Other:  |
| 9. <input type="checkbox"/> Cross-Cross Hatching Objectionable.                   |  |
| 10. <input type="checkbox"/> Double-Line Hatching Objectionable.                  |  |
- B. ☒ The drawings, submitted on 4/24/08, are so informal they cannot be corrected. New drawings are required. Submission of the new drawings MUST be made in accordance with the attached letter.

PIF 00039



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund

Group Art Office 253

Serial No.: 87/041,994

Examiner: J. Jackson

Filed : 04-24-87

Attorneys Docket No.:  
88-528-01

For : HIGH VOLTAGE MOS TRANSISTORS

COMMISSIONER OF PATENTS  
& TRADEMARKS  
Washington, D.C. 20231

Date of this Paper:

April 7, 1988

#### AMENDMENT

In response to the U.S. Patent Office Action mailed December 7, 1987 (Paper No. 2), please amend this application as follows:

#### In the Specification

Page 1, line 26, change "of" to --on--;

Page 5, line 15, insert the following paragraph:

--It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or epi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one complimentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.--

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88

(Date of Deposit)  
Thomas E. Schatzel  
Attorney  
4/7/88

PIF 00040

Page 9, line 28, change "72" to --73--.

In the Claims

Cancel claims 1-5 and 8-18.

Add new claims 19-23 as follows:

19. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

a source contact connected to one pocket,

a drain contact connected to the other pocket,

an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region,

and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

PIF 00041

26.<sup>4</sup> The high voltage MOS transistor of claim 15 having one channel conductivity type in combination with a <sup>complementary</sup> complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.

27.<sup>5</sup> The high voltage MOS transistor of claim 15 combined on the same chip with a low voltage CMOS implemented device.

28.<sup>4</sup> The combination of claim 27 further including,  
 a <sup>complementary</sup> complementary high voltage MOS transistor, and  
 a <sup>complementary</sup> complementary low voltage CMOS implemented device on the same chip and isolated from each other.

29.<sup>7</sup> A high voltage MOS transistor comprising:  
 a semiconductor substrate of a first conductivity type having a surface,  
 a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,  
 a source contact connected to one pocket,  
 an extended source region of the second conductivity type extending laterally each way from the source contact pocket to <sup>positions</sup> surface-adjoining positions,  
 a <sup>surface adjoining</sup> layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,  
 said top layer and said substrate being subject to application of a reverse-bias voltage,  
 a drain contact connected to the other pocket,

1) an extended drain region of the second conductivity type  
 extending laterally each way from the drain contact pocket to  
 surface-adjoining positions,  
 2) a <sup>surface adjoining</sup> layer of material of the first conductivity type on top of  
 an intermediate portion of the extended drain region between the  
 drain contact pocket and the surface-adjoining positions,  
 3) said top layer of material and said substrate being subject  
 to application of a reverse-bias voltage,  
 4) an insulating layer on the surface of the substrate and  
 covering at least that portion between the nearest surface-adjoining  
 positions of the extended source region and the extended drain region,  
 and  
 5) a gate electrode on the insulating layer and electrically  
 isolated from the <sup>substrate</sup> region thereunder which forms a channel laterally  
 between the nearest surface-adjoining positions of the extended source  
 region and the extended drain region, said gate electrode controlling  
 by field-effect the current flow thereunder through the channel.

Amend the claims as follows:

Claim 6, line 1, change "5" to --19--; and

Claim 7, line 1, change "5" to --19--.

#### REMARKS

The specification has been amended to correct minor errors and to provide an antecedent basis in the specification for epitaxial layer and epi-island mentioned in former claims 11 and 13.

This invention relates to high voltage, metal oxide semiconductor transistors of the field effect type. There is a need for more efficient transistors which can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The

PIF 00043

integrated devices should be easily combined with low voltage (five volt) control logic on the same chip. Devices of opposite conductivity should be combinable in a complimentary manner on the same chip. Such transistors, with modifications, should be capable of source-follower applications.

The applicant has disclosed a novel and unobvious high voltage MOS transistor having a low threshold voltage that is compatible with five volt control logic and a low ON-resistance. This transistor can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The high voltage MOS transistors can be modified for source-follower applications by providing both extended source regions and extended drain regions. These transistors are formed on a substrate of a first conductivity type having a surface. A pair of laterally spaced pockets of semiconductor material of a second conductivity type are provided within the substrate and adjoining the substrate surface. A source contact is connected to one pocket and a drain contact is connected to the other pocket. An extended drain region of a second conductivity type extends laterally each way from the drain pocket to surface-adjoining positions. A layer of material of the first conductivity type is provided on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The top layer of material and the substrate are subject to application of a reverse-bias voltage. None of the cited references show such structure.

Colak, U.S. Patent No. 4,626,879, shows a DMOS transistor suitable for source follower applications. This device has a substrate with three epitaxial layers formed thereon. A surface-adjoining channel region is diffused into the epitaxial layers and a source region is diffused into the channel diffusion above the channel region. A drain region is diffused into the top epitaxial layer. An extended drain

region is formed from a portion of the top epitaxial layer between the drain region and the channel region. The top and bottom epitaxial layers are interconnected, and the bottom layer may operate as a parallel extended drain region between the connection points. The intermediate epitaxial layer may operate as an extended drain region in a dual-gate/dual-drain structure wherein all three epitaxial layers contribute to device conductivity for achieving optimum normalized "ON" resistance.

Thomas, U.S. Patent No. 4,628,341 shows an integrated circuit structure that includes both low-voltage n-channel and p-channel MOS transistors and high voltage n-channel and p-channel MOS transistors.

The claims are now clearly distinguished from the cited references. New claim 19 recites "an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions, a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions". When high voltage n-channel and p-channel devices are combined on the same chip with low voltage control logic, this structure isolates the devices from each other. Claim 19 also provides for a pair of laterally spaced source and drain contact pockets within the substrate as is customary for conventional MOS transistors and is thus, distinguished from DMOS devices which require a higher threshold voltage. The structure of claim 19 enables a lower threshold voltage, compatibility with five volt control logic, and eliminates the need for an additional power supply and interface circuit.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and thus, can be distinguished for the same reasons as claim 19.

Claim 23 is directed to the transistor, shown in Fig. 5 of the drawings, that has been modified for source-follower applications by providing both extended source and drain regions. Top layers cover intermediate portions of the extended source and drain regions. The top layers and substrate are subject to application of a reverse-bias voltage.

Accordingly, claims 6-7 and 20-23 are patentably distinct from the cited references and allowance of these claims is requested.

If the Examiner is of the opinion that a telephone conference with applicant's attorney would expedite matters, such a conference is invited.

Respectfully submitted,

Reg. No. 22,611

By Thomas E. Schatzel  
Thomas E. Schatzel

LAW OFFICES OF THOMAS E. SCHATZEL  
A Professional Corporation  
3211 Scott Boulevard, Suite 201  
Santa Clara, California 95054  
Telephone: (408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Wash.

ington, D.C. 20231, on 4-7-88  
(Date of Deposit)

THOMAS E. SCHATZEL

Thomas E. Schatzel  
Signature Date

PIF 00046



Case Docket No. SS-821-01  
Date April 7, 1988

In re application of: **Klas H. Eklund**  
Serial No.: **07/041,994**  
Filed: **April 24, 1987**  
For: **HIGH VOLTAGE MOS TRANSISTORS**

COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

- ☐ No additional fee is required. ☒ Two Month Extension Fee Enclosed. (\$85.00)  
☐ Additional fee calculated as follows:

CLAIMS AS AMENDED					
	Claims remaining after amendment		Highest number previously paid for	Preheat extra	Rate
Total Claims		None	-	x	\$12.00
Indep. Claims		None	-	x	\$34.00

Additional Fee Due \$ \_\_\_\_\_

- ☒ A verified statement claiming small entity status. ☒ has been filed; \_\_\_\_\_ is attached. The fee due is fifty percentum of the above.  
Fee Due \$ \_\_\_\_\_  
☒ A check in the amount of \$ 85.00 is attached. (Two Month Extension)  
☒ Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

040 04/13/88 041994  
Attorney For Applicant

Law Offices of THOMAS E. SCHATZEL  
A Professional Corporation  
3211 Scott Boulevard Suite 201  
Santa Clara, CA 95054  
(408) 727-7077

By: Thomas E. Schatzel  
Reg. No.: 22,611

I hereby certify that the correspondence is being deposited with the United States Patent Service as that due and is in proper address for the Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88

Thomas E. Schatzel  
Signature Thomas E. Schatzel Date 4/7/88

PIF 00047

Serial No.: 97/041,994  
Filed: 04-24-87  
Attys. Docket No.: SS-520-01

PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

\_\_\_ other than a small entity

\_\_\_ verified statement attached

X small entity

X verified statement already filed

Payment of fees

X The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please \_\_\_ also charge issues fees under 37 C.F.R. 1.18  
X do not  
to Account No. 19-0310.

Reg. No. 22,611

*Thomas E. Schatzel*  
Attorney for Applicant

Telephone: (408) 727-7077

Law Offices of Thomas E. Schatzel  
A Professional Corporation  
3211 Scott Boulevard, Suite 201  
Santa Clara, California 95054

I hereby certify that this correspondence is being deposited with the United States Postal Service on first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Wash.

ington, D.C. 20231, on 4-7-88

Thomas E. Schatzel

*Thomas E. Schatzel*  
7/7/88  
Date

PIF 00048



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/871,994	04/24/87	ENLLIND	K SS-520-81

THOMAS E. SCHATZEL  
3211 SCOTT BLVD., STE. 201  
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR, J	
ART UNIT	PAPER NUMBER
253	4

DATE MAILED:

06/17/88

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been extended ☒ Responsive to communication filed on 4/11/88 ☒ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part 1 THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- |  |   |
|--|---|
| 1. <input checked="" type="checkbox"/> Notice of Relevance Cited by Examiner, PTO-892. | 2. <input type="checkbox"/> Notice re Patent Drawing, PTO-448.                  |
| 3. <input type="checkbox"/> Notice of Apt Cited by Applicant, PTO-148                  | 4. <input type="checkbox"/> Notice of Informal Patent Application, Form PTO-152 |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474     | 6. <input type="checkbox"/> _____   |

Part 2 SUMMARY OF ACTION

1. ☒ Claims 6, 7, 19-23 are pending in the application.  
Of the above, claims \_\_\_\_\_ are withdrawn from consideration.
2. ☐ Claims \_\_\_\_\_ have been cancelled.
3. ☐ Claims \_\_\_\_\_ are allowed.
4. ☒ Claims 6, 7, 19-23 are rejected.
5. ☐ Claims \_\_\_\_\_ are objected to.
6. ☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on \_\_\_\_\_. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed addition or substitute sheet(s) of drawings, filed on \_\_\_\_\_ has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed \_\_\_\_\_, has been ☐ approved; ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received; ☐ not been received.  
☐ been filed in parent application, serial no. \_\_\_\_\_, filed on \_\_\_\_\_.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1933 C.R. 11; 453 O.G. 213.
14. ☐ Other \_\_\_\_\_

PTOL-326 (Rev. 7-83)

EXAMINER'S ACTION

PIF 00049

Serial No. 041,994

-2-

Art Unit 253

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 171(c) of this title before the invention thereof by the applicant for patent.

Claims 19, 6, 7 are rejected under 35 U.S.C. 102

(e) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak.

Claim 19 still does not distinguish over Colak.

See figures 1, 2B and 2C of Colak where 22 and 24 define "pockets", layers 18 and 14 form an "extended drain" which extends to the surface "each way" from the drain contact 24, layer 16 defines a layer of material of first conductivity type "on top of" extended drain layer 14, and layer 16 and substrate 12 are subject to application of a reverse bias voltage during operation of the device. Note that layer 16 is connected to the source and the substrate is reverse biased through SS. Thus claim 19 does not distinguish over Colak. Claim 5 is undistinguishing since Colak teaches a layer 16 thickness of 2 micron for 400 V operation, however, for lower voltage operation design layer 16 would be thinner, and 1 micron thickness is thus an obvious design variant to the artist. Similarly, to the artist, the design of claim 7 is obvious in view of Colak who teaches  $10^{16}/\text{cm}^3$  for layer 16.

PIF 00050

Serial No. 041,994

-3-

Art Unit 253

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 20-23 are rejected under 35 U.S.C. 103 as being unpatentable over Colak in view of Thomas.

As stated in the previous rejection, Thomas shows that high voltage fet devices (as Colak) are advantageously formed complementary and also integrated with low voltage devices. Hence claims 20-22 are obvious.

Claim 23 is rejected under 35 U.S.C. 103 as being unpatentable over Sze.

Colak teaches punch through and avalanche protection layer 16 for a DMOS device. To one of ordinary skill it would have been obvious to practice the teachings of Colak in other MOS devices as ordinary fets as shown in Sze. Note figures 3, 51 or 52 of Sze where the source or drain are structurally similar and their function is dependent on the particular voltage applied. Hence, to the artist it would be obvious to apply the

PIF 00051

Serial No. 041,994

-4-

Art Unit 253

teachings of Colak to symmetrical ordinary fets as shown in 6ze to provide higher voltage operation.

Applicant's arguments filed April 11, 1988 have been fully considered but they are not deemed to be persuasive.

Applicant's argument that Colak does not show a drain "extending laterally each way" from the drain is not convincing as shown in the above rejection.

Clearly there is drain material 18 on each side of pocket 24.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, THIS ACTION IS MADE FINAL. See MPEP 706.07(a).

Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION PURSUANT TO 37 CFR 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Jackson whose telephone number is (703) 557-4824.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 557-3311.

J. Jackson:klw

6-15-88

(703) 557-4824

  
SUPERVISORY EXAMINER  
GROUP ART UNIT 253

PIF 00052

TO SEPARATE, 1/4" D TOP AND BOTTOM EDGES, SNAP-APART AND K. CARD CARBON

DRAFTED SET (REV. 3-78)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 041994	GROUP ART UNIT 253	ATTACHMENT TO PAPER NUMBER 4	
NOTICE OF REFERENCES CITED				APPLICANT Ehlund			
U.S. PATENT DOCUMENTS							
	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE	
A							
B							
C							
D							
E							
F							
G							
H							
I							
J							
K							
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT INTL. I. P. CLASS. SYST.
L							
M							
N							
O							
P							
Q							
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)							
R	See, Physics of Semiconductor Devices						
S	Wiley, New York, ©1981 pp 431-438, 486-491						
T							
U							
EXAMINER J. Jackson				DATE 6/88			
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)							

PIF 00053



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
87/8412, 994	84/24/87	EKLUND	K SS-528-81

THOMAS E. SCHATZEL  
3211 SCOTT BLVD., STE. 281  
SANTA CLARA, CA 95051-3893

EXAMINER	
JACKSON JR., J.	
ART UNIT	PAPER NUMBER
253	5

DATE MAILED:

#### EXAMINER INTERVIEW SUMMARY RECORD

08/11/88

All participants (applicant, applicant's representative, PTO personnel):

(1) Jack Edwards (2) Klas H. Eklund  
(3) Thomas E. Schatzel (4) Jerome Jackson

Date of interview: 10 August 1988

Type: ☒ Telephone ☐ Personal (copy is given to ☐ applicant ☐ applicant's representative)

Exhibit shown or demonstration conducted: ☐ Yes ☒ No. If yes, brief description:

Agreement: ☒ was reached with respect to some or all of the claims in question. ☐ was not reached.

Claims discussed: all

Identification of prior art discussed: Colak

Description of the general nature of what was agreed to if an agreement was reached, or any other comments: New amendments to the claims to be submitted distinguishing applicant's channel structure and surface adjoining legs 27 over Colak.

(A fuller description, if necessary, and a copy of the amendments, if available, which the examining agent would render the claims allowable must be attached. Also, where no copy of the amendments which would render the claims allowable is available, a summary thereof must be attached.)

Unless the paragraphs below have been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW in 4, Items 1-7 on the reverse side of this form, if a response to the last Office action has already been filed, then applicant is given one month from this interview date to provide a statement of the substance of the interview.

☐ It is not necessary for applicant to provide a response stated of the substance of the interview.

☐ Since the examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action.

PTOL-412 (Rev. 1-88)

Examiner's Signature

*Jerome Jackson Jr.*

ORIGINAL FOR INSERTION IN RIGHT HAND FLAP OF FILE WRAPPER

PIF 00054

88  
9/88

6/15/88  
R.A.

PATENT

8-15-88

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant : Klas H. Eklund  
Serial No.: 07/041,994  
Filed: : April 24, 1987  
For : HIGH VOLTAGE MOS TRANSISTORS

Group Art Unit: 253  
Examiner: J. Jackson, Jr.  
Attorneys Docket No.:  
58-528-01

**ATTENTION: BOX A.F.**

COMMISSIONER OF PATENTS  
& TRADEMARKS  
Washington, D.C. 20231

Date of this Paper:  
August 12, 1988

AMENDMENT AFTER FINAL

In response to the U.S. Patent Office Action mailed June 17, 1988  
(Paper No. 4), please amend this application as follows:

In the Claims

Claim 19, line 12, before "layer" insert --surface adjoining--;  
line 22, before "region" insert --substrate--.

Claim 20, line 2, change "complimentary" to --complementary--.

Claim 22, line 2, change "complimentary" to --complementary--;  
line 3, change "complimentary" to --complementary--.

Claim 23, line 9, delete "a";

~~line 10, change "position" to --positions--;~~

line 11, before "layer" insert --surface adjoining--;

line 18, delete "a";

line 20, before "layer" insert --surface adjoining--;

line 30, before "region" insert: ~~substrate~~.

REMARKS

The applicant appreciates the telephone interview on August 10, 1988, courteously granted by the Examiner.

Claim 19, as amended, now provides for an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions and a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The layer 16 of Colak is not surface-adjoining but is buried under layer 18. There is no layer of material of the first conductivity type on top of layer 18. Colak's layer 16 extends from beneath the drain contact pocket 24 to the channel region 20, and thus, is not between the drain contact pocket and the surface adjoining positions of the extended drain region.

Claim 19 also provides for the top layer of material and the substrate being subject to application of a reverse-bias voltage. Thus, the top layer and the substrate act as gates for controlling current flow through the extended drain region between the surface adjoining positions and the drain contact pocket. This structure can be considered a double-sided, junction-gate field-effect transistor (JFET). Colak shows a layer 14 intermediate a layer 16 and a substrate 12 that are subject to application of a reverse-bias voltage. Though this structure of Colak could be considered a double-sided JFET, layer 16 is not surface-adjoining as defined in claim 19. Colak's double-sided JFET is buried under layer 18 which is connected in parallel with layer 14 by semiconductor zones 15c, 16d. Layer 16 also acts as a gate for layer 18 so that layers 16 and 18 could be considered a single-sided JFET. Thus, the extended drain of Colak includes the single-sided JFET connected in parallel with the double-

sided JFET thereunder. Both the extended drain structure of claim 19 and Colak's drain structure have relatively high voltage capability. However, it is desirable to control the high voltage with relatively low voltage.

Claim 19 further provides for a substrate having a surface, an insulating layer on the surface of the substrate covering at least that portion between the source contact pocket and the nearest surface-  
adjoining position of the extended drain region, and a gate electrode on the insulating layer electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region. Thus, claim 19 is limited to a MOS or MOSFET structure, while Colak shows a D-MOS device. The MOSFET structure has a lower threshold voltage than a D-MOS device (0.7 volts compared to two - four volts for the D-MOS device) and thus, is directly compatible with five volt logic. D-MOS devices usually require an additional power supply of ten to fifteen volts for driving the gate. The MOSFET structure has less on-resistance and thus, further reduces the total on-resistance of the combined structure (MOSFET plus double-sided JFET).

Claim 19 is directed to the structural combination of a double-sided JFET and a MOSFET so that a high voltage transistor can be controlled with relatively low voltage. Thus, claim 19 is patentably distinct over Colak.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and are thus patentably distinct from Colak for the same reasons as claim 19. While Thomas shows that high voltage FET devices are advantageously formed complementary and also integrated with low voltage devices, claims 20-22 are limited to transistors having the structure as defined in claim 19. This structure facilitates isolation of complementary high voltage devices and low voltage, C-MOS

implemented devices on the same chip. Isolation of the epitaxial layers shown by Colak from corresponding layers of a complementary device would be difficult.

Claims 6 and 7 include further limitations on the depth of the top layer and the doping density thereof. The depth is one-half or less than that disclosed by Colak for layer 16 and the doping density is at least five times greater. Furthermore, Colak's layer 16 is not similarly situated as the top layer of claim 19, and thus, is not comparable. Thus, claims 6 and 7 are patentably distinct from Colak for the same reasons as claim 19 and for the further limitations therein.

Claim 23 is directed to the transistor 63, shown in Fig. 5, that is suitable for source follower applications. This claim contains limitations similar to claim 19 for the MOSFET structure and the double-sided JPET about the drain contact pocket. It further includes structural limitations for a double-sided JPET about the source contact pocket. While the book by Sze discloses MOSFET structures having sources and drains that are similar to each other, such sources and drains are not similar to the double-sided JPET structures disclosed by the applicant and specifically claimed structurally in claim 23. Thus, claim 23 is patentably distinguished from Sze.

Should the Examiner be of the opinion that a telephone conference with applicant's attorney would be beneficial, he is invited to contact the undersigned at the number set out below.

Respectfully submitted,

Reg. No. 22,611

By

  
Thomas E. Schatzel

LAW OFFICES OF THOMAS E. SCHATZEL  
A Professional Corporation  
3211 Scott Boulevard, Suite 201  
Santa Clara, California 95054  
Telephone: (408) 727-7077

PATENT

HAND CARRIED TO PTO

Case Docket No. SS-528-01Date August 12, 1988

In re application of: Klas N. Eklund  
 Serial No.: 07/041,994  
 Filed: April 24, 1987  
 For: HIGH VOLTAGE MOS TRANSISTORS

ATTN: BOX A-F  
 COMMISSIONER OF PATENTS AND TRADEMARKS  
 Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment After Final for the above application.

☒ No additional fee is required.

☐ Additional fee calculated as follows:

CLAIMS AS AMENDED						
	Claims remaining after amendment		Highest number previously paid for	Present extra	Rate	Admtl. Fee
Total Claims	_____	Times	_____ =	_____ x	\$12.00	= _____
Indep. Claims	_____	Times	_____ =	_____ x	\$34.00	= _____

Additional Fee Due \$ \_\_\_\_\_

☒ A verified statement claiming small entity status ☒ has been filed; \_\_\_\_\_ is attached. The fee due is fifty percent of the above.

Fee Due \$ \_\_\_\_\_

☐ A check in the amount of \$ \_\_\_\_\_ is attached.

☒ Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

Attorney For Applicant

By *Kahay*  
Reg. No.: 22,611

Law Offices of THOMAS E. SCHATZEL  
 A Professional Corporation  
 3211 Scott Boulevard Suite 201  
 Santa Clara, CA 95054  
 (408) 727-7077

PIF 00059

PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

\_\_\_ other than a small entity

\_\_\_ verified statement attached

x small entity

x verified statement already filed

Payment of fees

x The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please \_\_\_ also charge issues fees under 37 C.F.R. 1.10  
x do not  
to Account No. 19-0310.

Reg. No. 22,611

  
Attorney for Applicant

Telephone: (408) 727-7077

Law Offices of Thomas E. Schatzek  
A Professional Corporation  
3211 Scott Boulevard, Suite 201  
Santa Clara, California 95054

PIF 00060



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20530

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,593	05/24/07	EXLIND	K SE-520-01

THOMAS E. SCHWITZEL  
3211 SCOTT BLVD., STE. 201  
SANTA CLARA, CA 95051-3093

EXAMINER	
JACKSON, JR., J	
ART UNIT	PAPER NUMBER
253	7

DATE MAILED:

8-25-08  
08/25/08

### NOTICE OF ALLOWABILITY

#### PART I

- ☒ This communication is responsive to Amendment 15 8/15/08
- ☒ All the claims being allowed, PROSECUTION ON THE MERITS IS FOR PRACTICAL PURPOSES CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
- ☒ The allowed claims are 6, 7, 19-23
- ☐ The drawings filed on \_\_\_\_\_ are acceptable.
- ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received, ☐ not been received. ☐ been filed in parent application Serial No. \_\_\_\_\_, filed on \_\_\_\_\_.
- ☐ Note the attached Examiner's Amendment.
- ☐ Note the attached Examiner Interview Summary Record, PTO-413.
- ☐ Note the attached Examiner's Statement of Reasons for Allowance.
- ☐ Note the attached NOTICE OF REFERENCES CITED, PTO-800.
- ☐ Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

#### PART II

A SHORTENED-STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.302(b).

- ☐ Make the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
- ☒ APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
  - ☒ Drawing informality are indicated on the NOTICE RE PATENT DRAWINGS, PTO-646, attached hereto or to Paper No. 2. CORRECTION IS REQUIRED.
  - ☐ The proposed drawing correction filed on \_\_\_\_\_ has been approved by the examiner. CORRECTION IS REQUIRED.
  - ☐ Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
  - ☐ Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE DATES NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

#### Attachments

- |  |   |
|--|---|
| - Examiner's Amendment                       | - Notice of Informal Application, PTO-152 |
| - Examiner Interview Summary Record, PTO-413 | - Notice of Patent Drawings, PTO-646      |
| - Reasons for Allowance                      | - Listing of References Cited             |
| - Notice of References Cited, PTO-800        | - Other                                   |
| - Information Disclosure Citation, PTO-1449  |   |

*[Signature]*  
SUPERVISORY PATENT  
GROUP 1 UNIT 7

PTOL-37 (REV. 1-05)

USCIB4100 10-2004

PIF 00061

PTOL-95 (Rev. 1-88)


**UNITED STATES DEPARTMENT OF COMMERCE**  
**Patent and Trademark Office**

 Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
 Washington, D.C. 20231

**NOTICE OF ALLOWANCE  
 AND ISSUE FEE DUE**
**THOMAS E. SCHATZEL**  
**3211 SCOTT BLVD., STE. 201**  
**SANTA CLARA, CA 95054-3893**

 All communications regarding this  
 application should give the serial  
 number, date of filing, name of  
 applicant, and batch number.

 Please direct all communications  
 to the Attention of "OFFICE OF  
 PUBLICATIONS" unless advised  
 to the contrary.

 The application identified below has been examined and found allowable  
 for issuance of Letters Patent. PROSECUTION ON THE MERITS IS CLOSED.

SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
07/841,994	04/24/87	887	JACKSON JR, J	253 08/25/88
For Revised Applicant	EXLIND,	KLAS H.		

 TITLE OF  
 INVENTION **HIGH VOLTAGE MOS TRANSISTORS**

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPL. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
SB-528-81	357-046.000	L66	UTILITY	YES	\$280.00	11/25/88

The amount of the issue fee is specified in 37 C.F.R. 1.18. If the applicant qualified for and has filed a verified statement of small-entity status in accordance with 37 C.F.R. 1.27, the issue fee is one-half the amount for non-small entities. The issue fee due printed above reflects applicant's status as of the time of mailing this notice. A verified statement of small entity status may be filed prior to or with payment of the issue fee. However, in accordance with 37 C.F.R. 1.26, failure to establish status as a small entity prior to or with payment of the issue fee precludes payment of the issue fee in the amount so established by small entities and precludes a refund of any portion thereof paid prior to establishing status as a small entity.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE as indicated above. The application shall otherwise be regarded as ABANDONED. The issue fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or prior party in interest as shown by the records of the Patent and Trademark Office. Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of the notice of allowance, the issue fee is charged to the deposit account at the time of mailing of this notice in accordance with 37 C.F.R. 1.511. If the issue fee has been so charged, it is indicated above.

In order to minimize delays in the issuance of a patent based on this application, this Notice may have been mailed prior to completion of final processing. The nature and/or extent of the remaining action or processing requirements may cause slight delays of the patent. In addition, if prosecution is to be continued, this Notice of Allowance will be vacated and the appropriate Office action will follow in due course. If the issue fee has already been paid and prosecution is requested, the applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a deposit account.

In the case of each patent issuing without an assignment, the complete post office address of the inventor(s) will be printed in the patent heading and in the Official Gazette. If the inventor's address is now different from the address which appears in the application, please fill in the information in the space provided on PTOL-95b enclosed. If there are address changes for more than two inventors, send the additional addresses on the reverse side of the PTOL-95b.

The appropriate space in the ASSIGNMENT DATA section of PTOL-95b must be completed in all cases. If it is desired to have the patent issue to an assignee, an assignment must have been previously submitted to the Patent and Trademark Office or must be submitted not later than the date of payment of the issue fee as required by 37 C.F.R. 1.534. Where there is an assignment, the assignee's name and address must be provided on the PTOL-95b to ensure its inclusion in the printed patent.

Advance orders for 10 or more printed copies of the prospective patent can be made by completing the information in Section 4 of PTOL-95b and submitting payment therefor. If use of a deposit account is being authorized for payment, PTOL-95c should also be forwarded. The order must be for at least 10 copies and must accompany the issue fee. The copies ordered will be sent only to the address specified in section 1 or 1A of PTOL-95b.

☒ Have attached communication from the Examiner.

☐ This notice is issued in view of applicant's communication filed

**IMPORTANT REMINDER**

 Patents issuing on applications filed on or after Dec. 12,  
 1980 may require payment of maintenance fees. See 37 C.F.R.  
 1.20 (a)-(c).

**PATENT AND TRADEMARK OFFICE COPY**
**PIF 00062**

357 46

KLAS HEKLUND  
SS-520-01

Date of Allowance: 08/25/88  
Issue Date: 156  
Pat. No.: 07/041,994  
Filed: 04/24/87

U.S. Patent Mar. 7, 1989 Sheet 1 of 2 4,811,075

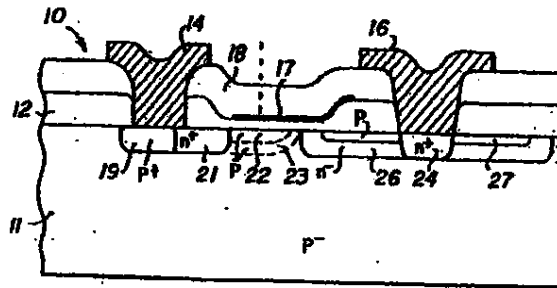


Fig. 1

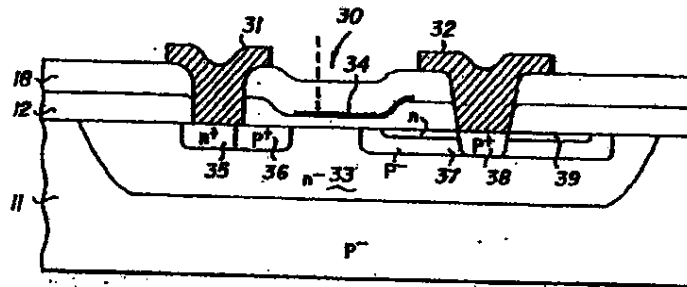


Fig. 2

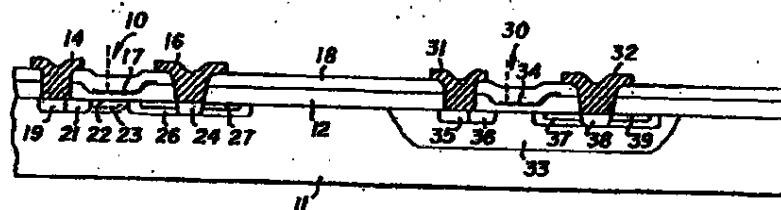


Fig. 3

PIF 00063

SS-520-01

**Pried**

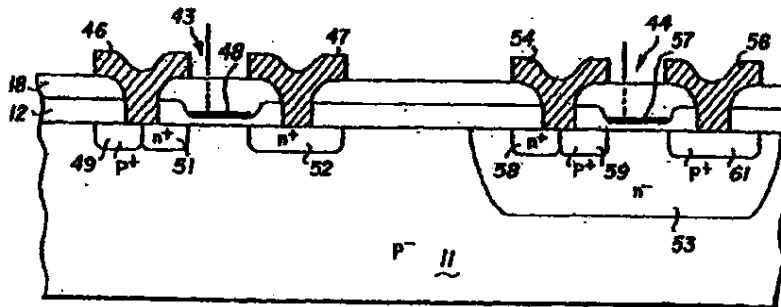
04/24/87

## U.S. Patent

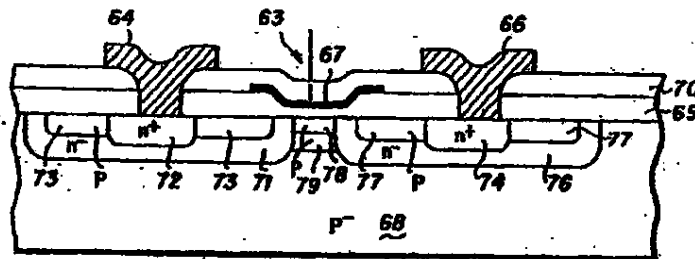
Mar. 7, 1989

Sheet 2 of 2

**4,811,075**



**Fig.4**




**Fig.5**

PIF 00064

Patent 7-8  
11-10-88

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Eklund, Kl<sup>ss</sup> H.  Issue Batch No.: L66  
Filed : 04/24/87 Allowance Date 08/25/88  
Examiner : Jackson Jr., Serial No. : 07/041,994  
Group Art Unit : 253  
Atty Docket No.: SS-520-01  
For : "HIGH VOLTAGE MOS TRANSISTORS"

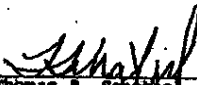
Box Issue Fees  
COMMISSIONER OF PATENTS  
AND TRADEMARKS  
Washington, D. C. 20231

Date of This App<sup>o</sup> 63  
OCT 31 AM 8:30  
RECEIVED  
PATENT & TRADEMARK OFFICE  
MAILING BRANCH  
October 19, 1988

FORMAL DRAWING TRANSMITTAL

Transmitted herewith are formal drawings for the above identified application as requested in the Notice of Allowance, Paper No. 7, mailed August 25, 1988. Corrections have been made as requested by the Examiner. Applicant respectfully requests that the formal drawings be filed.

Respectfully submitted,

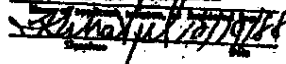
By:   
Thomas E. Schatzel  
Reg. No. 22,614

Attorney for Applicant

LAW OFFICES OF THOMAS E. SCHATZEL  
A Professional Corporation  
3211 Scott Boulevard, Suite 201  
Santa Clara, CA 95054-3093

Telephone: (408) 727-7877

I hereby certify that this correspondence is being deposited with the United States Postal Service in that class mail is so envelope addressed for the Commissioner of Patents and Trademarks, Wash-  
ington, D.C. 20231, on 10/19/88

THOMAS E. SCHATZEL  
  
10/19/88

PIF 00065

Applicant or Patentee: Klas H. Eklund Attorney's  
 Serial or Patent No.: 07/041,994 Docket No. 86-520-01  
 Filed or Issued: 04/24/87  
 For: "HIGH VOLTAGE MOS TRANSISTORS"

VERIFIED STATEMENT (REGISTRATION) CLAIMING SMALL ENTITY STATUS  
 (37 CFR 1.27(c)) - SMALL BUSINESS CONCERN

I hereby declare that I am

- ☐ the owner of the small business concern identified below;  
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN POWER INTEGRATIONS, INC.  
 ADDRESS OF CONCERN 411 Clyde Avenue  
Mountain View, CA 94043

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled "HIGH VOLTAGE MOS TRANSISTORS" by inventor(s)  
Klas H. Eklund

described in

- ☐ the specification filed herewith  
☒ application serial no. 07/041,994, filed April 24, 1987  
☐ patent no. \_\_\_\_\_, issued \_\_\_\_\_

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). \*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME N/A

ADDRESS

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

NAME N/A

ADDRESS

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Klas H. Eklund  
 TITLE OF PERSON OTHER THAN OWNER Vice President, Engineering  
 ADDRESS OF PERSON SIGNING Power Integrations, Inc., 411 Clyde Avenue,  
Mountain View, California 94043  
 SIGNATURE [Signature] DATE 4/24/88

PIF 00066

180 U.S. DEPT. OF COMMERCE  
Patent and Trademark Office

ISSUE FEE TRANSMITTAL

This form is part of a formal transmittal and should be used for transmitting the Issue Fee, Section 15A through 15D, to the Patent and Trademark Office.

INVENTOR'S NAME: JOHN E. SCHATTEL SERIAL NO. 07/041,777

INVENTOR'S ADDRESS: 24 1988

Street Address: 24

City, State and ZIP Code: 24

CO-INVENTOR'S NAME: JOHN E. SCHATTEL

Street Address: 24

City, State and ZIP Code: 24

☐ Check if additional charges are on reverse side

2A. The COMMISSIONER OF PATENTS AND TRADE-MARKS is requested to apply the Issue Fee to the application identified below.

2B. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will be printed.

1. LAW OFFICES OF THOMAS E. SCHATTEL  
2. A Prof. Corporation  
3.

SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
07/041,777	04/29/87	007	JACKSON JR, J	253 09/25/88

ATTY'S DOCKET NO.	CLASS/SUBCLASS	BATCHING	APPL. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
00-020-01	307-046.000	L66	UTILITY	YES	\$200.00	11/25/88

1A. Further correspondence is to be mailed to the following:  
Law Offices of THOMAS E. SCHATTEL  
A Professional Corporation  
3211 Scott Boulevard, Suite 201  
Santa Clara, California 95054

2B. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will be printed.

1. LAW OFFICES OF THOMAS E. SCHATTEL  
2. A Prof. Corporation  
3.

DO NOT USE THIS SPACE

040 10/28/88 04/1994 1 262 / 200.00 CA/  
040 10/28/88 04/1994 1 581 15.00 CA

2. ASSIGNMENT DATA (date or type)

A. ☐ This application is NOT assigned.  
☐ Assignment previously submitted to the Patent and Trademark Office.  
☐ Assignment submitted herewith.

B. For Printing On The Patent: (list an assignee as identified below, no assignee data will appear on the patent. Inclusion of assignee data below is only appropriate when an assignment has been previously submitted to the PTO or is submitted herewith. Completion of this form is NOT a substitute for filing of an assignment as required by 37 C.F.R. 1.334.)

(1) NAME OF ASSIGNEE: KLAH INNOVATIONS, INC.

(2) ADDRESS: 1000 S. State St. Corvallis, Oregon 97331

(3) STATE OF INCORPORATION, IF ASSIGNEE IS A CORPORATION: California

4. The following fees are enclosed: Ch. 1 11177  
☒ Issue fee ☒ Advanced order ☐ Assignment recording  
The following fees should be charged to deposit acct. no. 19-8310  
☐ PTO-450 or additional copy of PTO-450 must be enclosed  
☐ Issue fee ☐ Assignment recording  
☐ Advanced order ☒ Any additional fees due  
Number of advanced order copies required: 10  
(must be for 10 or more copies)

5. All correspondence relating to maintenance fees will be addressed to the correspondence address unless a separate "Fee Address" is provided to the Patent and Trademark Office (37 C.F.R. 1.363). A "Fee Address" may be submitted by the owner of record with the payment of the issue fee or thereafter by using form PTO-1537.

TRANSMIT THIS FORM WITH FEE

PIF 00067



Patent

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Eklund, Klas M.                      Issue Batch No.: 166  
 Filed : 04/24/87                                      Allowance Date 08/25/88  
 Examiner : Jackson Jr., J.                      Serial No. : 87/041,994  
 Group Art Unit : 253  
 Atty Docket No.: SS-528-01  
 For : "HIGH VOLTAGE MOS TRANSISTORS"

Box Issue Fees  
 COMMISSIONER OF PATENTS  
 AND TRADEMARKS  
 Washington, D. C. 20231

Date of This Paper

October 19, 1988

PAYMENT OF ISSUE FEE (37 CFR 1.311)

1. Applicant hereby pays the issue fee.
2. Fee (37 CFR 1.18(a))

Application status is:

☒ small entity-                                      fee \$ 200.00  
☒ Verified Statement attached  
☐ Verified Statement filed  
☐ other than small entity-                                      fee \$ 560.00

## 3. Payment of fee

☒ Enclosed please find check 11177 for \$ 302.00 .  
☐ Charge Deposit Account 19-0310 the sum  
 of \$ \_\_\_\_\_. A duplicate of this request  
 is attached.

\* Includes Advance Order and Assignment Recordal Fee

Respectfully submitted,

*Thomas E. Schatzel*  
 Thomas E. Schatzel  
 Reg. No. 22,611

Attorney for Applicant

Law Offices of THOMAS E. SCHATZEL  
 A Professional Corporation  
 3211 Scott Boulevard, Suite 201  
 Santa Clara, CA 95054-3093  
 Telephone: (408) 727-7077

I hereby certify that the foregoing is a true and correct copy of the original as filed with the United States Patent Service and that it is in accordance with the provisions of the Patent and Trademark Act, U.S.C. 2011, as amended.

10/19/88  
 Thomas E. Schatzel  
*Thomas E. Schatzel*

PIF 00068



Atty. Docket No.: SS-510-01 #70

POWER OF ATTORNEY BY ASSIGNEE

undersigned, as Assignee of the entire right, title, and interest in and to the subject matter which is described and claimed and for which a patent is sought on the invention entitled:

HIGH VOLTAGE MOS TRANSISTORS

the specification of which

☐ is attached hereto;

☒ was filed on April 24, 1987 as Application Serial No. 07/041,994 and was amended on 04/11/88; 08/15/88; (if applicable).

Assignment recorded on \_\_\_\_\_ at Real/Frame \_\_\_\_\_ (if applicable)

hereby elects to control the prosecution of this application and hereby appoints the following attorneys(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office in connection therewith:

Thomas E. Schatzel Reg. No. 22,611

Address all correspondence to:

LAW OFFICES OF THOMAS E. SCHATZEL  
A Professional Corporation  
3211 Scott Boulevard, Suite 201  
Santa Clara, California 95054-3093

Address all telephone calls to Thomas E. Schatzel at telephone No. (408) 727-7077.

Assignee hereby petitions and requests that this file be closed to the inventor(s), or representative(s) thereof.

POWER INTEGRATIONS, INC.

Dated: 11/18/88

by [Signature]  
Klaus H. Eklund

Title: Vice President, Engineering

POWER INTEGRATIONS, INC.  
411 Clyde Avenue  
Mountain View, California 94043

PIF 00069



U.S. DEPARTMENT OF COMMERCE  
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

Page No. 11

3 JAN 1989

253 4/24/87 04/1994  
Karl H. Eklund  
High Voltage MOS Transistors

This is in response to the communication re the Power of Attorney filed 10/24/88

- assignee
1. ☐ The power of attorney to you in this application has been revoked by the applicant.
2. ☐ In view of the notice in this application of the death of \_\_\_\_\_  
his power of attorney is terminated.
3. ☒ The power of attorney to you in this application has been accepted by the Commissioner of Patents and Trademarks.

For Record, Applicant

4. ☐ The assignee in this application has intervened and appointed an attorney of his own selection. Further correspondence will be held with said attorney. (Rule 36, Rules of Practice.)
5. ☐ The revocation of the power of attorney to \_\_\_\_\_ has been  
notified and said attorney has been notified. Further correspondence will be addressed to you.
6. ☐ On \_\_\_\_\_, the applicant appointed \_\_\_\_\_  
as additional attorney in this application. Further correspondence will continue to be addressed to you as  
specified in the new power of attorney.
7. ☐ On \_\_\_\_\_, the applicant appointed \_\_\_\_\_  
as additional attorney in this application. Further correspondence will be addressed to said attorney. MPEP 401.02
8. ☐ The complete power of attorney to you in this application has been revoked by the attorney of record.

Thomas E. Schatzel

Law Office of Thomas E. Schatzel  
Attorney at Law  
216 West 1st St., Ste 201  
San Jose, CA 95133-3773

L. E. Smith

RETAIN THIS COPY IN THE APPLICATION FILE

Copy A

FORM PTO-305 (REV. 8/78)

PIF 00070



THOMAS E. SCHATZEL  
16400 LARK AVENUE, STE. 300  
LOS GATOS, CA 95032

20-01

160

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 4,811,075

PATENT MAINTENANCE  
DIVISION

Granted: 03/07/89

Inventor(s): Klas H. Sklund

Dom Patent Address Change  
Commissioner of Patents and Trademarks  
Washington, D.C. 20231

ENTERED BY PMD (12)

7/04/994

## CHANGE OF CORRESPONDENCE ADDRESS IN PATENT

Please

1. Change the address of the attorney(s) of record to:

Thomas E. Schatzel, Esq.  
LAW OFFICES OF  
THOMAS E. SCHATZEL  
A PROFESSIONAL CORPORATION  
16400 LARK AVENUE, SUITE 300  
LOS GATOS, CA 95032

2. Change the correspondence address of the patent owner to:

It is certified that the person whose signature appears below has the authority to change  
the correspondence address for the patent.

Date: 05/03/93

LAW OFFICES OF  
THOMAS E. SCHATZEL  
A PROFESSIONAL CORPORATION  
16400 LARK AVENUE, SUITE 300  
LOS GATOS, CA 95032

Tel. No.: (408) 369-7730

Reg. No.: 22,611

(if applicable)

(Signature)

THOMAS E. SCHATZEL

☐ Inventor(s)☐ Assignee of complete interest☒ Attorney or agent of record

I hereby certify that this correspondence is true  
deposited with the United States Postal Service as  
first class mail in an envelope addressed to the  
Commissioner of Patents and Trademarks, Wash.  
ington, D.C. 20231, on 05/03/93  
(Date of Deposit)

THOMAS E. SCHATZEL

Signature

(Change of Correspondence Address in Patent [15-8])

PIF 00071

PATENT APPLICATION SERIAL NO. **041994**

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE  
FEE RECORD SHEET

050 04/30/87 041994

1 201 170.00 CX

PIF 00072

FORM PTO-875 REV. 4-98	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO. <b>041994</b>	FILED DATE <b>APR 24, 1987</b>
PATENT APPLICATION FEE DETERMINATION RECORD		APPLICANT FIRST NAME <b>Edo H. Eklund</b>	

## CLAIMS AS FILED - PART I

FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
POTENTIAL CLAIMS	<b>18</b>	<b>-20 = 0</b>
INDEF. CLAIMS	<b>3</b>	<b>-3 = 0</b>
IF INDEFINITE DEPENDENT CLAIMS PRESENT		

\* If the difference in col. 1 is less than zero, enter "0" in col. 2.

## SMALL ENTITY

RATE	FEE
	\$150
x10=	\$
x15=	\$
x20=	\$
x25=	\$
TOTAL	<b>\$170</b>

OTHER THAN A  
SMALL ENTITY

RATE	FEE
	\$300
x10=	\$
x15=	\$
x20=	\$
x25=	\$
TOTAL	\$

## CLAIMS AS AMENDED - PART II

AMENDMENT A	(1) CLAIMS REMAINING AFTER AMENDMENT	(2) HIGHEST NO. PREVIOUSLY PAID FOR	(3) PRESENT EXTRA
	<b>7</b>	<b>20</b>	
	<b>2</b>	<b>3</b>	
IF FIRST PRESENTATION OF MULTIPLE DEP. CLAIMS			

## SMALL ENTITY

RATE	ADDITIONAL FEE
	\$
x10=	\$
x15=	\$
x20=	\$
x25=	\$
TOTAL	\$

OTHER THAN A  
SMALL ENTITY

RATE	ADDITIONAL FEE
	\$
x10=	\$
x15=	\$
x20=	\$
x25=	\$
TOTAL	\$

AMENDMENT B	(1) CLAIMS REMAINING AFTER AMENDMENT	(2) HIGHEST NO. PREVIOUSLY PAID FOR	(3) PRESENT EXTRA
	<b>7</b>	<b>20</b>	
	<b>2</b>	<b>3</b>	
IF FIRST PRESENTATION OF MULTIPLE DEP. CLAIMS			

RATE	ADDITIONAL FEE
	\$
x10=	\$
x15=	\$
x20=	\$
x25=	\$
TOTAL	\$

RATE	ADDITIONAL FEE
	\$
x10=	\$
x15=	\$
x20=	\$
x25=	\$
TOTAL	\$

AMENDMENT C	(1) CLAIMS REMAINING AFTER AMENDMENT	(2) HIGHEST NO. PREVIOUSLY PAID FOR	(3) PRESENT EXTRA
IF FIRST PRESENTATION OF MULTIPLE DEP. CLAIMS			

RATE	ADDITIONAL FEE
	\$
x10=	\$
x15=	\$
x20=	\$
x25=	\$
TOTAL	\$

RATE	ADDITIONAL FEE
	\$
x10=	\$
x15=	\$
x20=	\$
x25=	\$
TOTAL	\$

\* If the entry in Col. 1 is less than the entry in Col. 2, enter "0" in Col. 3.

\*\* If the "Highest No. Previously Paid For" in THIS SPACE is less than 20, enter "20".

\*\*\* If the "Highest No. Previously Paid For" in THIS SPACE is less than 3, enter "3".

The "Highest No. Previously Paid For" (found as above) is the highest number found in the appropriate box in Col. 2.

PIF 00073

**PIF 00074**

ORIGINAL CLASSIFICATION	
CLASS 357	SUBCLASS 46
CROSS REFERENCES	
CLASS 357	22 23.9 23.8
APPLICANT'S NAME PLEASE PRINT Eklund	
INTERNATIONAL CLASSIFICATION (INT. CL. 4)	
H01L	27/02
A01L	29/78
H01L	29/80
GROUP AND UNIT 253	ASSISTANT EXAMINER PLEASE STAMP OFFICER FULL NAME Jerome Jackson Jr. PRIMARY EXAMINER PLEASE STAMP ON FRONT PAGE NAME NORMAN L. MOSES
ISSUE CLASSIFICATION SUPERVISORY PAY - U.S. DEPT. OF COMMERCE GROUP ART UNIT 253	

## INDEX OF CLAIMS

Claim	Date
1	
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(770001)

☐ Request  
☐ Amendment  
☐ Withdrawal  
☐ Surrender  
☐ Appeal  
☐ Opposition  
☐ Revocation  
☐ Opposition  
☐ Appeal  
☐ Opposition  
☐ Appeal

PIF 00075

Handwritten signature: *K. J. [unclear]*

SEARCH NOTES		
	Date	Exms.

**PX 19**



*With their high input impedance, fast switching, and low losses, power MOSFETs simplify the design of off-line switching-mode power supplies. One controller IC can drive the FETs directly.*

## Power MOSFETs take the load off switching supply design

Until recently, switching power supplies were fabricated primarily with fast bipolar devices. Now, the advent of the power MOSFET is making possible switching-mode supplies that are simpler, smaller, less expensive, more efficient, and in particular easier to design.

A MOSFET can be driven directly from an IC switching-mode controller-regulator chip without intervening power amplification. Moreover, it lends itself to the trouble-free design of a family of supplies by requiring only minor adjustments in drive circuitry when changing from one output voltage and current rating to another. A bipolar power device, on the other hand, may require not only greatly different component values but also a totally different drive circuit for differently rated members of the same power supply family.

The power MOSFET simplifies supply design primarily because of its high input impedance. This factor makes possible a full-power output with very low drive current. Thus a single driver-circuit configuration can easily drive one or more power MOSFETs having a wide range of output power capability to produce a family of regulated supplies. In contrast, a supply using bipolar transistors would generally require different driver circuits for different power levels, because the bipolar transistor's power output

is a direct function of its base drive.

However, though the power MOSFET's gate consumes virtually no current under steady-state conditions, it does require power while switching on and off, because the gate-to-drain and gate-to-source self-capacitance must be charged and discharged fast enough to obtain the desired switching speed. The drive circuit must therefore have a sufficiently low output impedance to supply the required charging and discharging current. But even under those conditions, a MOSFET's drive circuit needs negligible average current when compared with an equivalent bipolar unit (Fig. 1).

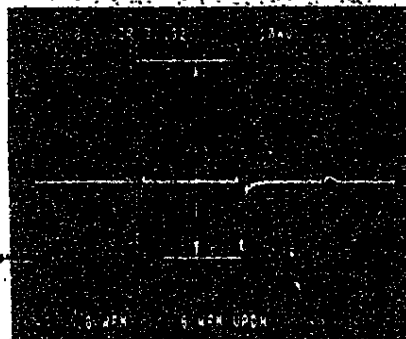
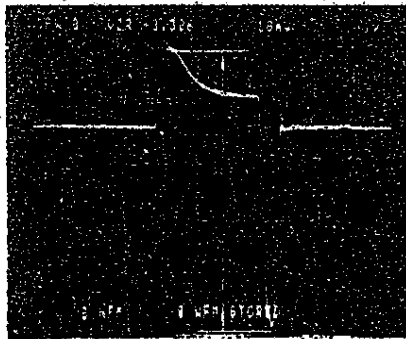
Also, a switching supply built with a power

## COMPONENTS SPECIAL

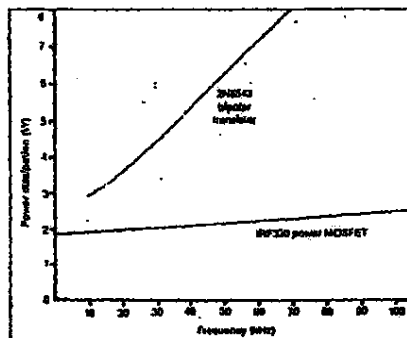
MOSFET is simpler than one using a bipolar transistor because the MOSFET does not exhibit the secondary breakdown characteristic of a bipolar transistor, which limits its power rating at high collector-emitter voltages and requires protection circuits. In addition, a bipolar device's negative temperature coefficient can result in thermal runaway: localized current hogging can cause excessively high current in one small area of the chip, called a hot spot, and start the device on the road to self-destruction. The power MOSFET, however, has a positive temperature coefficient of its on-resistance, which prevents such runaway. Furthermore, the positive coefficient tends to effect an even distribution of current throughout the chip. Thus the device's full rated current at maximum rated

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## Components Special: Power MOSFETs



1. A bipolar transistor used in a switching regulator circuit requires significantly greater drive power than a comparably rated MOSFET. Waveforms are shown for a bipolar device (top) and a MOSFET (bottom), each switching 2.5 A and 270 V at 100 kHz. The vertical scales are 500 mA/division and 100 V/division, respectively.



2. Because switching losses are lower, the total losses in a power MOSFET are less than those in a similar bipolar device. These include both input drive requirements and saturation (on) losses.

voltage can generally be made the most of.

A further advantage of the power MOSFET is its high forward transconductance, which increases with increasing current, enabling it to handle high peak current. A bipolar device, in contrast, has a lower beta at high current and may actually pull out of saturation at the maximum load current, causing greater than expected dissipation.

## Higher switching speeds

The power MOSFET also switches faster than comparably rated bipolar transistors. That makes possible operation at a higher switching frequency. The higher speeds are possible because a MOSFET is not affected by minority-carrier delays that are inherent in the operation of bipolar devices. Instead, the switching time of a MOSFET is determined primarily by self-capacitance and circuit inductance. Typical switching times for power MOSFETs are 30 to 50 ns for devices rated at 400 V and 20 A peak; minimum switching speeds can be much faster, with 10 ns easily achievable. These speeds are about 10 times faster than those readily available from similarly rated bipolar transistors. High switching speeds enable a switching-mode power supply to use smaller magnetic elements, filter capacitors, and EMI filters, permitting the construction of a smaller supply—often at lower cost.

Though higher speeds are an easily understood advantage of MOSFETs, their better efficiency needs some explanation: A MOSFET's usually higher on-state voltage drop might indicate greater overall power loss than that exhibited by comparable bipolar devices. However, that is generally not the case, because the total dissipation, which includes both the loss in the on-resistance and the switching losses, must be considered.

Switching loss in a bipolar transistor is generally the major loss component. It is much higher than the switching loss in a MOSFET. Therefore, although the on-resistance loss may be high at dc at high switching frequencies, the total dissipation of the power MOSFET will at some frequency become less than that of a bipolar device.

The bipolar transistor also requires appreciable base drive, which means added dissipation in the external drive circuits. In addition, the bipolar unit always needs a snubber circuit (collector-emitter diode) to shape the dynamic load line and keep it within the safe operating area when switching.

A comparison of the losses associated with the power MOSFET and an equivalent power bipolar device is a key factor in the choice of which to use and at what frequency. A comparison between the two types, both operating at 270 V and 2.5 A is



3. A complete resonant high-frequency filter to produce regulator chip, pulse width of 1. The power output changing to a 10



4. An efficient, easy-to-use power MOSFET, a 2N



### Components Special: Power MOSFETs

shown in Fig. 2. It takes into account the on-state saturation loss, the drive circuit power, and the switching losses of both devices and clearly indicates the superior efficiency of the MOSFET.

To see the efficiency and simplicity of switching-mode supply design using MOSFETs, consider the circuit shown in Fig. 3. In this off-line forward converter, the 115-V power line is rectified and filtered to supply about 180 V dc to the MOSFET switch. Drive current for the power MOSFET is furnished directly by a pulse-width modulator-regulator that runs freely at 100 kHz. The secondary of the transformer is rectified and filtered to provide a nominal +5-V output. This voltage is also used as negative feedback and is applied to the error input of the modulator-regulator. The latter compares the +5-V input with an internal reference voltage and develops a difference voltage that controls the pulse width of the 100-kHz signal applied to the MOSFET through an isolating drive transformer. If the +5-V output of the supply changes, the pulse width of the power MOSFET drive signal changes in the opposite direction in order to keep the output of the supply constant.

The reservoir capacitor determines the amount of brownout protection provided by the supply, that is, how long the supply will maintain its output should its input power momentarily disappear due to a power-line transient.

#### All control functions

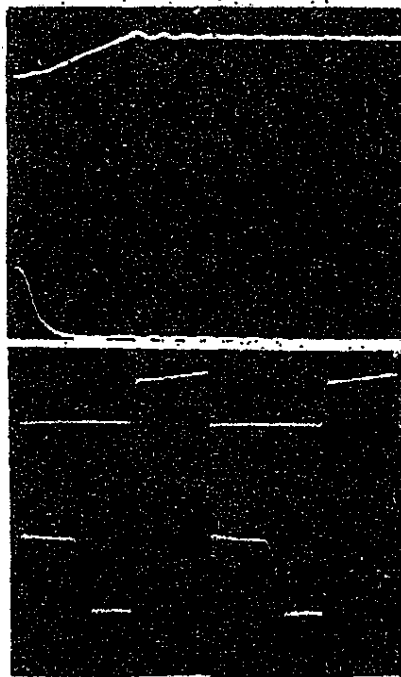
Figure 4 shows a detailed circuit diagram of a 100-W, +5-V, off-line supply using a power MOSFET switch operating at 100 kHz. Tables 1 and 2 summarize the supply's performance, giving the measured efficiency, typical input voltages, and load while the supply is switching at 100 and 200 kHz. The efficiency is virtually the same at both frequencies, indicating that the power MOSFET is still running below its maximum operating frequency. Changing from 100 to 200 kHz requires only reducing the timing resistor,  $R_{on}$ , of the SG3526 from 6.2 to 2 k $\Omega$ .

The typical performance of a power MOSFET in such a circuit is shown in the oscillograms (Fig. 5). Based on these oscillograms, it can be estimated that the energy dissipated at turn-on is about 0.0022 mJ, whereas at turn-off it is almost an order of magnitude greater—0.016 mJ. The difference occurs because the transformer leakage reactance slows the rate of rise of current at turn-on, minimizing the turn-on energy and stores energy that is subsequently dissipated during turn-off.

The total switching power dissipated by the MOSFET at 100 kHz is 1.8 W. That relatively low figure affords a switching efficiency of over 98%.

Table 1. How the 100-W off-line switching power supply performs

Minimum input voltage	95 V rms, 50–400 Hz
Maximum input voltage	130 V rms, 50–400 Hz
Output voltage	+5 V dc
Dc output voltage regulation for all conditions of output current and input voltage	$\pm 0.5\%$
Maximum output ripple voltage	50 mV pk-pk
Transient response for a step change of 10-A load current	100 mV, settling within 250 $\mu$ s
Full load efficiency	76%

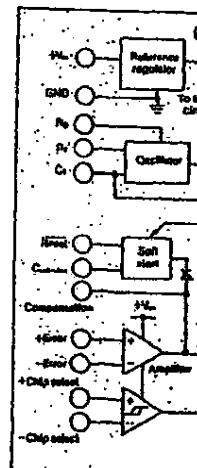


5. In the circuit of Fig. 4 the drain-current rise time of the power MOSFET (left top) is about 300 ns, and it is limited by transformer inductance. Leakage reactance slows the turn-on current. On the other hand, the drain voltage (left bottom) takes about 250 ns to stabilize. Cycle-by-cycle waveforms of drain current and drain voltage are shown at right top and bottom, respectively.

A single IC, the SG3526, forms all the control output capability for the MOSFET directly without a temperature, a sawtooth of pulse-width modulating logic, and two (Fig. 6). Also on the DIP, are protective (undervoltage lockout), pulse inhibition, metering, adjustable vision for symmetry. One of the totem-pole capacitors  $C_{out}$  (pin 13) drives the power MOSFET output (pin 16) output can continue as well as providing an

Table 2.

	Dc output voltage	
100 kHz	100 V	0
200 kHz	100 V	0



6. The SG3526, part of the SG3526 family, is used for single-ended or push-pull transformerless and transformer

A single IC, the Silicon General SG3526, performs all the control functions and has sufficient output capability to drive an IRP720 power MOSFET directly without a buffer stage in between. It contains a temperature-compensated voltage reference, a sawtooth oscillator, an error amplifier, a pulse-width modulator, pulse metering and steering logic, and two low-impedance power drivers (Fig. 6). Also on the chip, which comes in an 18-pin DIP, are protective features, such as soft start and undervoltage lockout, digital current limiting, double pulse inhibition, a data latch for single pulse metering, adjustable dead-time circuitry, and provision for symmetry correction inputs.

One of the totem-pole outputs of the SG3526 (pin 13) drives the power MOSFET's gate by means of capacitor  $C_g$ , transformer  $T_s$ , and resistor  $R_g$ . The other output (pin 16) is unused and left open. Either output can continuously sink and source 100 mA, as well as providing an output current of 200 mA peak.

This capability is more than adequate for any MOSFET switch capable of an output of up to 250 W.

Among the important features of the SG3526 is the undervoltage lockout circuit, which protects the device and the associated power MOSFET from an inadequate supply voltage. If the dc voltage is too low, the circuit disables the output drivers and holds the Reset pin low. That prevents spurious output pulses after the supply is turned on; during the time the control circuits are stabilizing, the circuit also holds the soft-start timing capacitor in a discharged state; the soft-start circuit in turn protects the power MOSFET and rectifier diodes from any possible high current surges. □

#### How useful?

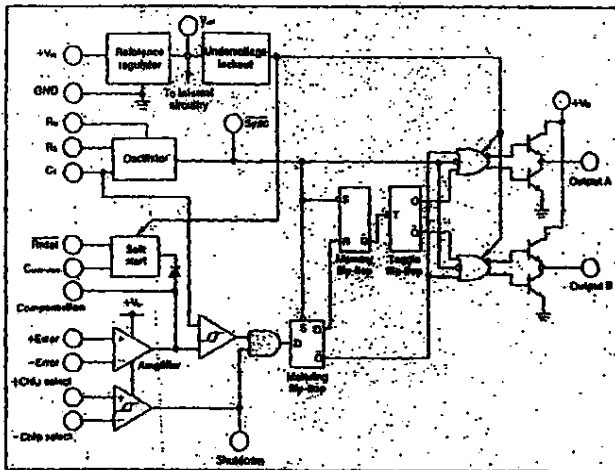
Immediate design application  
Within the next year  
Not applicable

Circle

547  
548  
549

Table 2: Comparing the supply's characteristics at 100 and 200 kHz

	Input source voltage	DC source current	DC power input	DC output voltage	DC output current	DC power output	Efficiency
100 kHz	160 V	0.832 A	133.12 W	5.83 V	19.38 A	100 W	75.1%
200 kHz	160 V	0.834 A	133.44 W	5.83 V	19.38 A	100 W	74.9%



4. The SG3526, part of the power supply shown in Fig. 4, combines the functions of a pulse-width modulator and a regulator for fixed-frequency switching supplies. It can be used for single-ended or push-pull regulators of positive and negative polarity, both transformerless and transformer-coupled.

**PX 29**

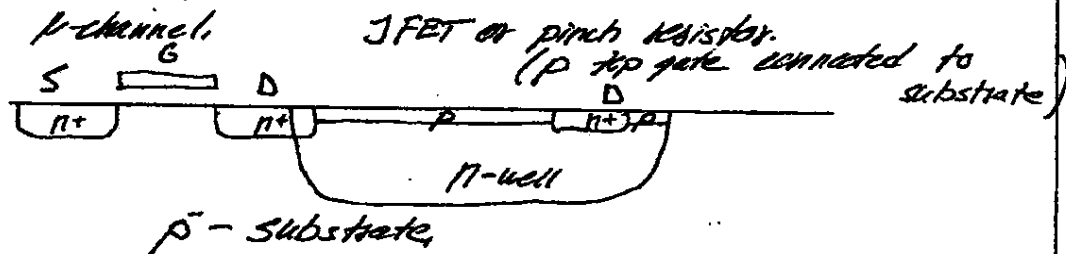
Klas. H. Ekland, 9/28-84

Increasing the operating voltage of a MOS transistor, by cascading a JFET (or pinch resistor) which for  $V_{ZD}$  takes up the increased voltage.

Example:

An n-well CMOS process, where the n-well forms the JFET.

The top gate p is formed by the field implant



JFET charac.

$$\left. \begin{array}{l} V_P = 5V. \\ N_D = 10^{16} \\ d = 1\mu m. \\ V_B > 100V. \end{array} \right\} \Rightarrow S/D = 2k\Omega/\mu$$

Case No. 04-1371-JJF

PX-29

Date Entered: \_\_\_\_\_

By: \_\_\_\_\_

Transistor example;

Pin 80 volt transistor for 200 mA.

$$V_{sat} \leq 1V.$$

- MOS transistor size. (CS-5).  $S/D \approx 2k\Omega/\mu m$ .

$$V = 0.5V.$$

$$= 150 \times 200 \mu m^2$$

- JFET size. channel length =  $5 \mu m$ .  $V = 0.5V$ .

$$\text{total length} = 20 \mu m.$$

$$= 500 \times 200 \mu m^2$$

$$\Rightarrow \text{total size. } \underline{130,000 \mu m^2}.$$

to compare with a similar size

bipolar transistor. which is,  $180,000 \mu m^2$ .

### Breakdown Voltage

The p top gate implants will reduce the surface field so nearly the theoretical breakdown for a plane junction will be achieved.

The doping in the p substrate is typically  $\approx 8 \times 10^{14}$   $\Rightarrow V_B \approx 400V$ .

Size comparison. With MOS high voltage  
high current transistor.

- D-MOS vertical transistor.

$$\left. \begin{array}{l} I_A \\ V_{DS} = 1V. \end{array} \right\} \Rightarrow A = 1 \text{ mm}.$$

$$V_B = 100V. \quad (1EDM-83 \text{ Optimum Design of Power MOSFETS})$$

Scaling to 200 mA.

$$\Rightarrow A = 200,000 \mu\text{m}^2.$$

to compare with 130,000  $\mu\text{m}^2$ .

So the lateral device seems to be  
very good, even in comparison with  
a vertical D-MOS device

- D-MOS lateral transistor in combination with.

C-MOS logic.

$$\left. \begin{array}{l} 0.5A \\ V_{DS} = 15V. \end{array} \right\} (1EDM-83 \text{ A highly reliable } 16 \text{ output high voltage CMOS/PMOS logic})$$

$$V_B = 400V.$$

$$A = 16 \text{ mm}^2.$$

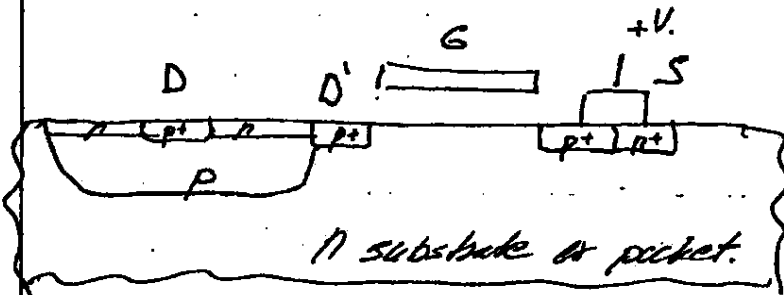
Scaling to 200 mA. and  $V_{DS} = 1V. \Rightarrow$

$$A = \frac{16 \times 15}{25} = 9.6 \text{ mm}^2.$$

to compare with 0.13  $\text{mm}^2$  for the

proposed lateral device.  
(For 400V, the channel length of the JFET.)  
Size has to be increased from 5  $\mu\text{m}$ .

The same concept may be used for a p-channel transistor used as a pull up device see figure below:



In this case one has to use a thicker gate oxide which will increase  $R_{on}$  for the p-channel device. But this will be about compensated by the high voltage on the drain. So this device should be about as efficient as the proposed n-channel device.

**PX 30**

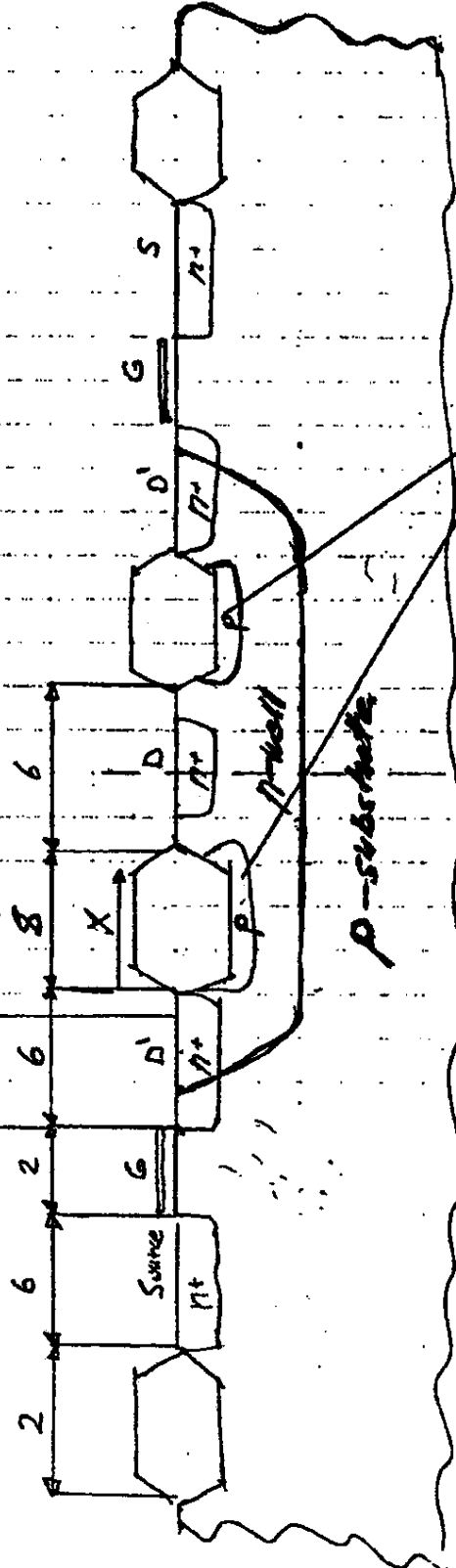
Edw. H. Eklund 1, -85

High voltage MOS device

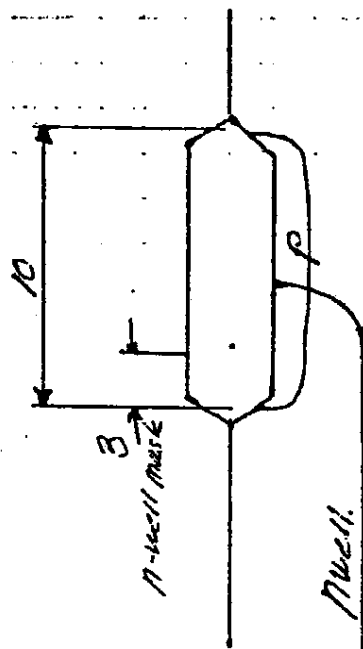
N-channel cascaded with pinch resistor

W = 100  $\mu$ m

S = 2, 3, 4, 6, 8 (5 devices)  
X = 2 (N-channel field implant)



N-channel field implant



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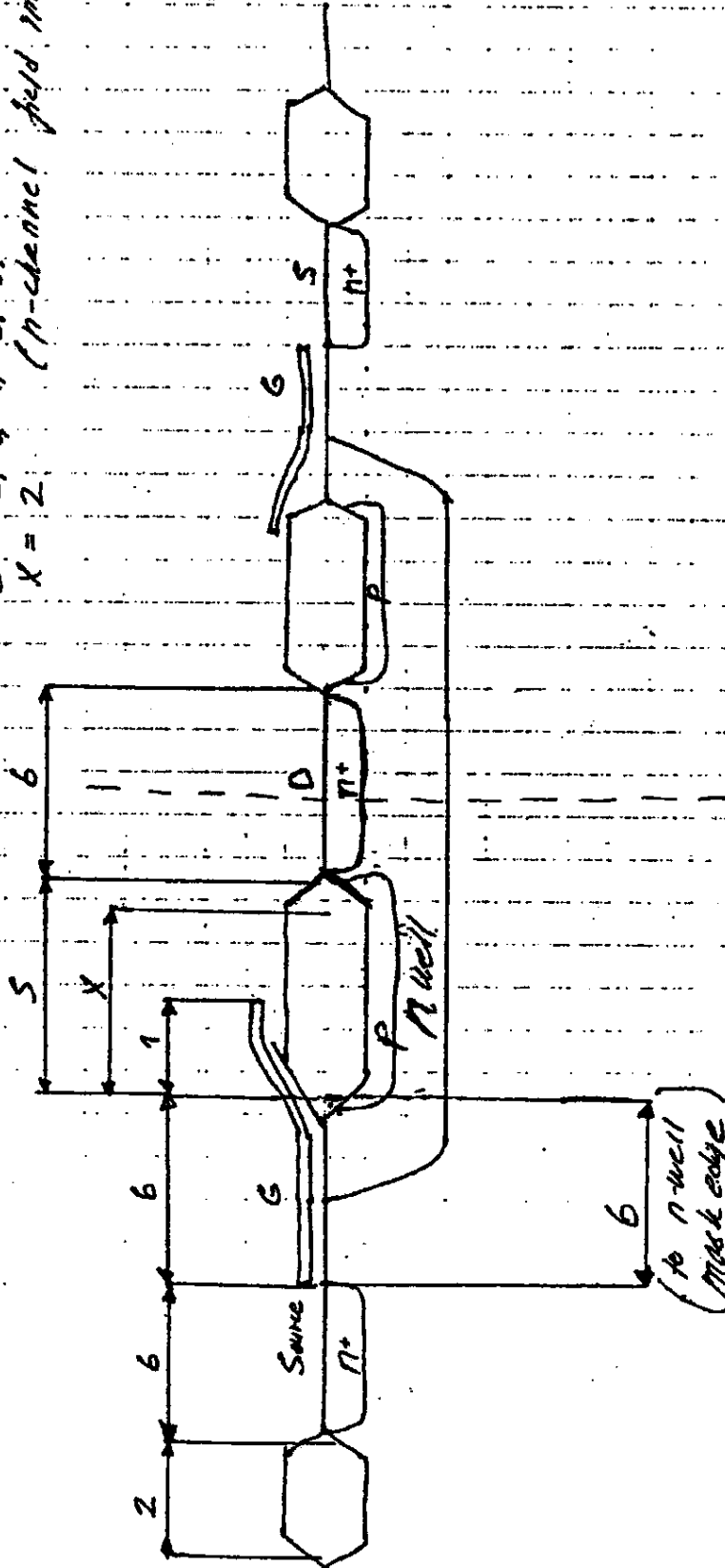
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High voltage MOS device

p-channel with n-well chain cascaded with pinch resistor

$S = 2, 3, 4, 6, 8$   
 $X = 2$  (p-channel field implant)



**PX 50**

**REDACTED**

**PX 56**